UNITED STATES PATENT AND TRADEMARK OFFICE
DOCUMENT CLASSIFICATION BARCODE SHEET

CATEGORY:

CLEARED

ADDRESS
CONTACT IF FOUND:

U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

B/O Form PTO-1390	Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under *35 USC 371*	*Attorney's Docket Number* JEK/Vater
		U.S. Application Number (if known) 09/700656
International Application Number PCT/EP99/03385	*International Filing Date* 17 May 1999	*Priority Date Claimed* 18 May 1998
Title of Invention ACCESS-CONTROLLED DATA STORAGE MEDIUM		
Applicant(s) for DO/EO/US Harald VATER et al.		

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items under *35 USC 371*:

1. ☒ This is a **FIRST** submission of items concerning a filing under *35 USC 371*.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under *35 USC 371*.
3. ☒ This express request to begin national examination procedures *(35 USC 371(f))* at any time rather than delay examination until the expiration of the applicable time limit set in *35 USC 371(b)* and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed *35 USC 371(c)(2)*.
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English *(35 USC 371(c)(2))*.
7. ☒ Amendments to the claims of the International Application under PCT Article 19 *(35 USC 371(c)(3))*
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 *(35 USC 371(c)(3))*.
9. ☒ An oath or declaration of the inventor(s) *(35 USC 371(c)(4))*. (☐ Executed ☒ Unexecuted)
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 *(35 USC 371(c)(5))*.

Items 11 to 16 below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under *37 CFR 1.97* and *1.98*.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with *37 CFR 3.28* and *3.31* is included.
13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: 4 sheets of formal drawings

532 Rec'd PCT/PTO 17 NOV 2000

Application Number (if Known)	International Application Number	Attorney's Docket Number
09/700656	PCT/EP99/03385	JEK/Vater

	Calculations	PTO USE ONLY
17. The following fees are submitted: **Basic National Fee *(37 CFR 1.492(a)(1)-(5))*:** ☒ Search report has been prepared by the EPO or JPO . . . . . $860.00 ☐ International Preliminary Examination Fee paid to USPTO *(37 CFR 1.482)* . . . . . $690.00 ☐ No International Preliminary Examination Fee paid to USPTO *(37 CFR 1.482)* but International Search Fee paid to USPTO *(37 CFR 1.445(a)(2))* . . . . . $710.00 ☐ Neither International Preliminary Examination Fee *(37 CFR 1.482)* nor International Search Fee *(37 CFR 1.445(a)(2))* paid to USPTO . . . . . $1000.00 ☐ International Preliminary Examination Fee paid to USPTO *(37 CFR 1.482)* and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT	**$ 860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date *(37 CFR 1.492(e))*.		

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	41 -20 =	21	× $18.00	$ 378.00	
Independent Claims	3 -3 =		× $80.00		
Multiple Dependent Claims (if applicable)			+ $270.00		
			TOTAL OF ABOVE CALCULATIONS	**$ 1,238.00**	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity Statements must also be filed (Note *37 CFR 1.9, 1.27, 1.28)*					
			SUBTOTAL	**$ 1,238.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date *(37 CFR 1.492(f))*.					
			TOTAL NATIONAL FEE	**$ 1,238.00**	
Fee for recording the enclosed assignment *(37 CFR 1.21(h))*. The assignment must be accompanied by an appropriate cover sheet *(37 CFR 3.28, 3.31)*. **$40.00** per property.					
			TOTAL FEES ENCLOSED	**$ 1,238.00**	
			Amount to be: Refunded:		
			Charged:		

a. ☒ A check in the amount of **$1,238.00** to cover the fees is enclosed.

b. ☐ Please charge my **Deposit Account Number 02-0200** in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account Number 02-0200**. A duplicate copy of this sheet is enclosed.

Note: Where an appropriate time limit under *37 CFR 1.494* or *1.495* has not been met, a petition to revive *(37 CFR 1.137(a) or (b))* must be filed and granted to restore the application to pending status.

BACON & THOMAS, PLLC
625 SLATERS LANE - FOURTH FLOOR
ALEXANDRIA, VIRGINIA 223124-1176
(703) 683-0500

DATE: 17 November 2000

Respectfully submitted,

J. ERNEST KENNEY
Attorney for Applicant
Registration Number: 19,179

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

International Patent Application
No. PCT/EP99/03385

PCT/DO/EO/US

International Filing Date: 17 May 1999

Applicant: Harald VATER et al.

For: ACCESS-CONTROLLED DATA STORAGE MEDIUM

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper accompanies documents submitted to establish the U.S. national stage of the above-identified international patent application.

The international patent application was amended under PCT Article 34 and the claims as-amended are annexed to the International Preliminary Examination Report (IPER).

Before calculation of the filing fee and before examination, kindly amend the claims as annexed to the IPER as follows:

IN THE CLAIMS:

Claim 3, line 1; change "either of the above claims" to --claim 1--;

Claim 4, line 1; change "any of the above claims" to --claim 1--;

Claim 5, line 1; change "any of the above claims" to --claim 1--;

Claim 7, line 1; change "either of claims 5 and 6" to --claim 5--;

Claim 10, line 1; change "any of claims 5 to 7" to --claim 5--;

Claim 11, line 1; change "any of claims 5 to 10" to --claim 5--;

Claim 12, line 1; change "any of claims 5 to 11" to --claim 5--;

Claim 13, line 1; change "any of the above claims" to --claim 1--;

Claim 15, line 1; delete "or 14";

Claim 16, line 1; delete "or 14";

Claim 17, line 1; change "either of claims 13 and 14" to --claims 13--;

Claim 18, line 1; change "any of claims 13 to 17" to --claim 13--;

Claim 19, line 1; change "any of claims 13 to 18" to --claim 13--;

Claim 20, line 1; change "any of the above claims" to --claim 1--;

Claim 21, line 1; change "any of the above claims" to --claim 1--;

Claim 24, line 1; change "either of claims 22 and 23" to --claim 22--;

Claim 25, line 1; change "any of claims 22 to 24" to --claim 22--;

Claim 28, line 1; change "either of claims 26 and 27" to --claim 26--;

Claim 31, line 1; change "any of claims 26 to 30" to --claim 26--;

Claim 32, line 1; change "any of claims 26 to 31" to --claim 26--;

Claim 33, line 1; change "any of claims 26 to 32" to --claim 26--;

Claim 36, line 1; delete "or 35";

Claim 37, line 1; delete "or 35";

Claim 38, line 1; change "either of claims 34 and 35" to --claim 34--;

Claim 39, line 1; change "any of claims 34 to 38" to --claim 34--;

Claim 40, line 1; change "any of claims 35 to 39" to --claim 35--;

Claim 41, line 1; change "any of claims 22 to 40" to --claim 22--;

REMARKS

All rights are reserved to the original claimed subject matter. The claims have been amended to reduce the filing fees and to correct any improper multiple dependent claims. Examination of the application as amended is respectfully requested.

Respectfully submitted,
BACON & THOMAS, PLLC

J. ERNEST KENNEY
Attorney for Applicant
Registration Number 19,179

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314
Telephone: (703) 683-0500
Facsimile: (703) 683-1080

Date: November 17, 2000
S:\Producer\jek\VATER - pct03385\preliminary amendment.wpd

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Harald VATER et al. | **Group Art Unit: unassigned PCT/DO/EO/US**

Serial No. 09/700,656 | **Examiner: unassigned**

Filing Date: 17 May 1999

For: ACCESS-CONTROLLED DATA STORAGE MEDIUM

SECOND PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Before examination on the merits, kindly amend this application in accordance with the following particulars:

IN THE SPECIFICATION:

Cancel the page entitled "new page 2A of description" if this amendment has been entered.

Page 1, between the third and fourth paragraphs; insert the following:

--US patent US-A-4,932,053 discloses a data carrier with semiconductor chips which has at least one memory in which an operating program containing a plurality of commands is stored. Each command causes signals detectable from outside the semiconductor chip. The signals are measured by current consumption at the terminals of the integrated circuit, permitting the processed data to be inferred. To prevent reading, a protection circuit is provided which generates a pseudorandom sequence by means of simulation cells. The current behavior which is measurable from outside is thus superimposed with a random signal.

French laid-open print FR-A-2 745 924 discloses making signals unrecognizable by using for a random generator which leads to desynchronization during execution of instruction sequences or program sequences within the processor.--

Serial No. 09/700,656

REMARKS

By way of this amendment, the amended sheet entitled "new page 2A of description" has been canceled from its location between pages 2 and 3 and has been moved between the third and fourth paragraphs on page 1 of the specification, in accordance with its intended location.

Examination of the application as amended is requested.

Respectfully submitted,
BACON & THOMAS, PLLC

J. ERNEST KENNEY
Attorney for Applicant
Registration Number 19,179

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314
Telephone: (703) 683-0500
Facsimile: (703) 683-1080

Date: February 14, 2001
S:\Producer\jek\VATER - 700656\preliminary amendment 2.wpd

Access-protected data carrier

This invention relates to a data carrier having a semiconductor chip in which secret data are stored. The invention relates in particular to a smart card.

Data carriers containing chips are used in a great number of different applications, for example for performing monetary transactions, paying for goods or services or as identification means for access or admission controls. In all such applications the chip of the data carrier normally processes secret data which must be protected from access by unauthorized third parties. Such protection is ensured by, among other things, giving the inner structures of the chip very small dimensions so that it is very difficult to access said structures with the aim of spying out data processed in said structures. In order to impede access further, the chip can be embedded in a very firmly adhering mass whose forcible removal destroys the semiconductor plate or at least the secret data stored therein. It is likewise possible to provide the semiconductor plate during its production with a protective layer which cannot be removed without destroying the semiconductor plate.

With corresponding technical equipment, which is extremely expensive but nevertheless fundamentally available, an attacker could possibly succeed in exposing and examining the inner structure of the chip. Exposure could be effected for example by special etching methods or a suitable grinding process. The thus exposed structures of the chip, such as conductive paths, could be contacted with microprobes or examined by other methods to determine the signal patterns in said structures. Subsequently one could attempt to determine from the detected signals secret data of the data carrier, such as secret keys, in order to use them for purposes of manipulation. One could likewise attempt to selectively influence the signal patterns in the exposed structures via the microprobes.

The invention is based on the problem of protecting secret data present in the chip of a data carrier from unauthorized access.

This problem is solved by the feature combinations of the independent claims.

The inventive solution, unlike the prior art, involves no measures to prevent exposure of the internal structures of the chip and the mounting of microprobes. In-

stead measures are taken to make it difficult for a potential attacker to infer secret information from any intercepted signal patterns. The signal patterns depend on the operations which the chip is performing. Said operations are controlled with the aid of an operating program stored in a memory of the chip. The operating program is composed of a series of individual commands each triggering an exactly specified operation. So that the chip can perform the intended functions a corresponding command string is to be defined for each of said functions. Such a function can be for example the encryption of data with the aid of a secret key. To give an attacker intercepting the processes on the chip by microprobes he has mounted as little information as possible about the particular commands executed and the data used in executing the commands, a desired function is preferably realized using commands of such a kind, or using commands in such a way, that it is difficult if not impossible to spy out information. In other words, no commands or command strings are to be used which allow the processed data to be inferred in a simple way by interception.

It is always especially easy to infer data when a command processes very few data, for example one bit. For this reason one preferably uses commands, according to an embodiment of the invention, which simultaneously process a plurality of bits, e.g. one byte, at least for all security-relevant operations, such as encryption of data. Such simultaneous processing of a plurality of bits blurs the influence the individual bits have on the signal pattern caused by the command into a total signal from which it is very difficult to infer the individual bits. The signal pattern is much more complex than in the processing of individual bits and it is not readily evident which part of the signal belongs to which bit of the processed data.

Additionally or alternatively, one can impede an attack on the processed data according to the invention by using in security-relevant operations solely commands which trigger an identical or very similar signal pattern or commands by which the processed data have very little or no influence on the signal pattern.

According to another advantageous embodiment of the invention, one performs security-relevant operations not with authentic secret data but with falsified secret data from which the authentic secret data cannot be determined without the addition of further secret information. This means that even if an attacker succeeds in deter-

New page 2a of description

US patent US-A-4,932,053 discloses a data carrier with semiconductor chips which has at least one memory in which an operating program containing a plurality of commands is stored. Each command causes signals detectable from outside the semiconductor chip. The signals are measured by current consumption at the terminals of the integrated circuit, permitting the processed data to be inferred. To prevent reading, a protection circuit is provided which generates a pseudorandom sequence by means of simulation cells. The current behavior which is measurable from outside is thus superimposed with a random signal.

French laid-open print FR-A-2 745 924 discloses making signals unrecognizable by using for a random generator which leads to desynchronization during execution of instruction sequences or program sequences within the processor.

mining the secret data used in an operation, he cannot cause any damage since the spied-out data are not the authentic secret data but falsified secret data.

In order to guarantee the functioning of the data carrier one must ensure that the data carrier delivers the right results when rightfully used despite the falsified secret data. This is obtained by first specifying a function for falsifying the authentic secret data, for example EXORing the secret data with a random number. The authentic secret data are falsified with the thus specified function. The falsified secret data are used to perform all those operations in the data carrier in which falsification of the secret data can subsequently be compensated. In the case of EXOR-falsified secret data, these would be operations which are linear with respect to EXOR operations. Before execution of an operation not permitting such compensation, for example an operation which is nonlinear with respect to EXOR operations, the authentic secret data must be restored so that said operation is performed with the authentic secret data. The authentic secret data are restored after execution of a compensable function for example by EXORing the function value determined by means of the falsified secret data with a corresponding function value of the random number used for falsification. It is important in this context for random number and function value to be previously determined and stored in safe surroundings so that the calculation of the function value from the random number cannot be intercepted.

The above procedure means that the authentic secret data are used only for performing operations, such as nonlinear operations, for which this is absolutely necessary, i.e. which cannot be performed alternatively with falsified secret data. Since such operations are normally very complex and not easy to analyze, it is extremely difficult if not impossible for a potential attacker to find out the authentic secret data from analyzing the signal patterns caused by said operations. Since the simply structured functions permitting subsequent compensation of falsification are performed with falsified secret data, the described procedure makes it extremely difficult to determine the authentic secret data of the data carrier from illegally intercepted signal patterns.

The signal patterns depend on the operations which the chip is executing. If said operations are always executed according to the same rigid pattern, i.e. in par-

ticular in the same order, and the attacker knows this order, an attacker need overcome much fewer difficulties to spy out data than if he does not even know which operation is being executed at which time. It is therefore provided according to a further embodiment of the invention to move as far away as possible from a rigid flow pattern when executing security-relevant operations within the smart card, thereby offering the attacker next to no hints for analyzing the secret data. This is obtained by executing as many operations as possible, ideally even all operations, which are independent of each other insofar as each of the operations requires no data determined by the other operations, in a variable order, for example one that is random or dependent on input data. This achieves the result that an attacker, who will normally be oriented by the order of the operations, cannot readily find out which operation is being executed. This holds especially when the operations resemble each other very strongly or are even the same with respect to the signal pattern they cause with the same input data. If the attacker does not even know the kind of operation which is being executed, it is extremely difficult to spy out data selectively. If there is the danger of an attacker making a great number of spying attempts in order to average out the random variation of the order, it is recommendable to make the variation dependent on the input data.

The invention will be explained below with reference to the embodiments shown in the figures, in which:

Fig. 1 shows a smart card from the front, and

Fig. 2 shows a greatly enlarged detail of the chip of the smart card shown in Fig. 1 from the front.

Fig. 3 shows a schematic representation of part of an operational sequence within the smart card, and

Fig. 4 shows a variant of the operational sequence shown in Fig. 3.

Fig. 5 shows a schematic representation of the sequence in the execution of some operations by the smart card.

Fig. 1 shows smart card 1 as an example of the data carrier. Smart card 1 is composed of card body 2 and chip module 3 set in a specially provided gap in card body 2. Essential components of chip module 3 are contact surfaces 4 via which an

electric connection can be made with an external device, and chip 5 electrically connected with contact surfaces 4. Alternatively or in addition to contact surfaces 4, a coil not shown in Fig. 1 or other transfer means can be present for producing a communication link between chip 5 and an external device.

Fig. 2 shows a greatly enlarged detail of chip 5 from Fig. 1 from the front. The special feature of Fig. 2 is that it shows the active surface of chip 5, i.e. Fig. 2 omits all layers which generally protect the active layer of chip 5. In order to obtain information about the signal patterns inside the chip one can for example contact exposed structures 6 with microprobes. The microprobes are very thin needles which are brought in electric contact with exposed structures 6, for example conductive paths, by means of a precision positioning device. The signal patterns picked up by the microprobes are processed with suitable measuring and evaluation devices in order to infer secret data of the chip.

The invention achieves the result that an attacker cannot gain access, or only with great difficulty, to in particular secret data of the chip even if he succeeds in removing the protective layer of chip 5 without destroying the circuit and contacting exposed structures 6 of chip 5 with microprobes or otherwise intercepting them. The invention is of course also effective if an attacker gains access to the signal patterns of chip 5 in another way.

According to the invention, the commands or command strings of the operating program of the chip are selected at least in all security-relevant operations in such a way that the data processed with the commands can either not be inferred at all or at least only with great difficulty from the intercepted signal patterns.

This can be achieved for example by fundamentally using in security operations no commands which process individual bits, such as the shift of individual bits, intended to cause a permutation of the bits of a bit string. Instead of bit commands one can use for example byte commands such as copy or rotation commands which process not an individual bit but a whole byte comprising eight bits. The byte command triggers a much more complex signal pattern than the bit command, it being extremely difficult to associate individual bits with partial areas of the signal pattern.

This blurs the information processed with the byte command, making it difficult to spy out said information.

Further, the invention offers the possibility of fundamentally using in security-relevant operations only commands triggering a very similar signal pattern so that it is very difficult to differentiate the commands being executed by the signal patterns. It is likewise possible to design the commands so that the kind of processed data has very little or no influence on the signal pattern triggered by the command.

The described variants can be used either alternatively or in combination with respect to the individual commands. An inventive set of security-relevant commands can thus be composed of commands belonging to one or more of the abovementioned variants. One can likewise use an instruction set in which all commands belong to the same variant, it also being allowed that some or all commands belong to other variants as well. For example, one can allow solely byte commands, preferably using those commands which in addition trigger a very similar signal pattern.

Security-relevant operations include e.g. encryption operations which are frequently used in smart cards. Such encryptions involve execution of a series of single operations which lead to bit-by-bit changes in a data word. According to the invention all these commands are replaced with byte commands and/or the abovementioned inventive measures are taken. This makes it even more difficult for an attacker to infer the secret keys used in encryption from the intercepted signal patterns, thereby preventing abuse of said secret keys.

Fig. 3 shows a schematic representation of part of an operational sequence in the smart card. An encryption operation was selected for the representation by way of example. However, the principles explained by this example are also applicable to any other security-relevant operations. At the onset of the part of the encryption operation shown in Fig. 3 data *abc*, which can be present in plaintext or already encrypted, are supplied to logic point 7. At logic point 7 data *abc* are combined with key $K1$. In the present example this combination is an EXOR operation but other suitable forms of combination can also be used. Nonlinear function g is then applied to the result of combination in function block 8. In order to show that function block 8 represents a nonlinear function it has the form of a distorted rectangle in Fig. 3.

The data produced with function block 8 are EXORed with random number Z at logic point 9 and subsequently processed in function block 10. Combination with random number Z causes falsification of the data which makes it difficult for an attacker to analyze the processes in function block 10 representing a linear mapping by means of function f. An undistorted rectangle is used as a symbol of a linear function in Fig. 3. The data produced in function block 10 are combined at logic point 11 with data $f(Z)$ previously generated e.g. during production of the card by application of function f to random number Z. This combination compensates the falsification of the data with random number Z at logic point 9. Said compensation is necessary since nonlinear function g is subsequently to be applied to the data in function block 12 and compensation of falsification is no longer possible after application of a nonlinear function to the data. Further, the data are EXORed at logic point 11 with key $K2$ which is necessary in connection with the encryption operation.

The combination at logic point 11 with the data $f(Z)$ and $K2$ can be effected either with single components $K2$ and $f(Z)$ or with the result of an EXOR operation of said components. The latter procedure opens up the possibility of key $K2$ not needing to be available in plaintext but only key $K2$ EXORed with $f(Z)$. If this combination value was calculated and stored in the memory of the card previously, e.g. during initialization or personalization of smart card 1, it is unnecessary to store key $K2$ in smart card 1 in plaintext. This further increases the security of smart card 1.

After application of function g to the data in function block 12 the thus determined result is in turn combined with random number Z at logic point 13 and thereby falsified. Linear function f is then applied to the result of combination in function block 14. Finally, the data are EXORed with the result of an application of function f to random number Z and with key $K3$ at logic point 15. This operation can be followed by further processing steps not shown in Fig. 3.

All in all, the procedure shown in Fig. 3 can be summarized by saying that the data processed in the encryption operation are falsified whenever possible by EXORing with random number Z in order to prevent secret data from being spied out. Falsification is fundamentally possible with all functions f showing linear behavior with respect to EXOR operations. With nonlinear functions g the unfalsified data

must be used. It is therefore necessary that the falsification be compensated by EX-ORing the data with function value $f(Z)$ before application of nonlinear function g to the data. It is less critical from a security point of view that nonlinear functions g can only be applied to the unfalsified data since said nonlinear functions g are much more difficult to spy out than linear functions f. The diagram shown in Fig. 3 is applicable both for identical functions g or functions f and for different respective functions.

The diagram shown in Fig. 3 achieves the result that it is almost impossible to spy out secret data during the processing of data *abc*. However, since upon provision of secret keys $K1$, $K2$ and $K3$ operations are also to be executed with said keys which could in turn be the target of a spying attempt by an attacker, it is recommendable to take corresponding safety precautions in the processing of the keys. An embodiment of the invention involving such safety precautions is shown in Fig. 4.

Fig. 4 shows a part corresponding to Fig. 3 of an operational sequence of a smart card for a further variant of the invention. Processing of data *abc* is identical to Fig. 3 and will therefore not be explained again in the following. In contrast to Fig. 3, however, keys $K1$, $K2$ and $K3$ are not supplied to logic points 7, 11 and 15 in Fig. 4. Instead, falsified keys $K1'$, $K2'$ and $K3'$ are supplied together with random numbers $Z1$, $Z2$ and $Z3$ required for compensating falsification, the falsified keys preferably being supplied first and then the random numbers. This ensures that proper keys $K1$, $K2$ and $K3$ do not appear at all. This procedure is especially advantageous in encryption methods by which keys $K1$, $K2$ and $K3$ are derived from common key K. In this case key K falsified with random number Z is stored in smart card 1, and random numbers $Z1$, $Z2$ and $Z3$ determined by application of the key derivation method to random number Z are stored in smart card 1. Storage must be done in safe surroundings, for example in the personalization phase of smart card 1.

For carrying out the functional diagram shown in Fig. 4 one requires not only the stored data but also falsified derived keys $K1'$, $K2'$ and $K3'$. Said keys can be derived from falsified key K when they are required. With this procedure no operations are performed with authentic key K or authentic derived keys $K1$, $K2$ and $K3$ so that it is virtually impossible to spy out said keys. Since derived random numbers $Z1$, $Z2$

and $Z3$ were also determined and stored in smart card 1 in advance, no more operations are performed therewith which could be spied out by an attacker. Thus, no access is possible to authentic derived keys $K1$, $K2$ and $K3$ by spying out falsified derived keys $K1'$, $K2'$ and $K3'$ since this requires derived random numbers $Z1$, $Z2$ and $Z3$.

In order to increase security further it is also possible to use a different random number Z for each EXOR operation, making sure that an $f(Z)$ is then also present for compensating the falsification in each case. In one embodiment, all random numbers Z and function values $f(Z)$ are stored in the memory of the smart card. However, it is likewise possible to store only a small number of random numbers Z and function values $f(Z)$ and determine new random numbers Z and function values $f(Z)$ by EXORing or another suitable combination of several stored random numbers Z and function values $F(Z)$ whenever said values are required. Random numbers Z can be selected for EXORing from the set of stored random numbers Z at random.

In a further embodiment, there is no storage of random numbers Z and function values $f(Z)$ since they are generated by means of suitable generators whenever required. It is important that the generator or generators do not generate function values $f(Z)$ by applying linear function f to random number Z but that pairs of random numbers Z and function values $f(Z)$ be generated in another way since random number Z might otherwise be spied out by interception of the application of function f to random number Z and further secret data determined with the aid of this information.

According to the invention, basically all security-relevant data, for example keys, can be falsified with the aid of further data, such as random numbers, and then be supplied to processing. This achieves the result that an attacker spying out said processing can only determine worthless data since they are falsified. At the end of processing the falsification is undone.

Fig. 5 shows a schematic representation of the sequence during execution of some operations by the smart card. Fig. 5 shows in particular which operations must necessarily be executed sequentially by smart card 1 since they depend on each other, and which operations can basically be executed in parallel and thus in any order. In this connection Fig. 5 shows part of a program run of smart card 1 in which

data *abc* are processed. All operations that have to be executed sequentially are shown sequentially in Fig. 5. All operations not requiring a special order of execution are disposed in parallel.

Processing of data *abc* begins with operation *P*1 shown in the form of block 70. The block is followed sequentially by block 80 representing operation *P*2. Fig. 5 thus indicates that the processing order of operations *P*1 and *P*2 cannot be interchanged, i.e. is obligatory. After block 80 the diagram shown in Fig. 5 branches into five blocks 90, 100, 110, 120, 130 representing operations *P*3, *P*4, *P*5, *P*6 and *P*7. It results that blocks *P*3, *P*4, *P*5, *P*6 and *P*7 can be executed simultaneously and thus also executed in any order. According to the invention the execution order of operations *P*3, *P*4, *P*5, *P*6, *P*7 is varied in each run, i.e. it is not foreseeable for an attacker which of said operations follows operation *P*2, which operations are performed after that, etc. Variation of the order can be effected either according to a fixed pattern or, better still, randomly or in accordance with input data by fixing by means of a random number or by the input data which of operations *P*3, *P*4, *P*5, *P*6 and *P*7 is executed next. This possibly random variation of the execution of the individual operations makes it difficult to spy out the data processed with the operations. When all operations *P*3, *P*4, *P*5, *P*6 and *P*7 are executed, operation *P*8 necessarily follows whose processing order is not variable. Operation *P*8 is shown by block 140. Operation *P*8 can be followed by further operations whose order is either variable or fixed, which are not shown in Fig. 5.

The invention can be used for example for the execution of encryption algorithms which frequently contain similar operations whose processing order is variable. The processing order can either be fixed before the first variable operation jointly for all operations interchangeable with said first operation, or the operation to be processed next can be determined before each variable operation from the set of remaining variable operations. In both cases one can use random numbers for fixing the processing order.

Patent claims

1. A data carrier with a semiconductor chip (5) having at least one memory in which an operating program containing a plurality of commands is stored, each command causing signals detectable from outside the semiconductor chip (5), characterized in that the data carrier (1) is designed to perform security-relevant operations solely executing operating program commands of such a kind, or executing said commands in such a way, that the data processed with the corresponding commands cannot be inferred from the detected signals.
2. A data carrier according to claim 1, characterized in that the commands used are designed for at least byte-by-byte processing of data.
3. A data carrier according to either of the above claims, characterized in that the commands used are indistinguishable with respect to the signal patterns caused thereby.
4. A data carrier according to any of the above claims, characterized in that the commands used each lead to a signal pattern which is substantially independent of the data processed with the command.
5. A data carrier according to any of the above claims, characterized in that the operating program is able to execute a series of operations (f), input data being required for executing the operations (f) and output data being generated by execution of the operations (f), whereby
   - the input data are falsified by combination with auxiliary data (Z) before execution of one or more operations (f),
   - the output data determined by execution of the one or more operations (f) are combined with an auxiliary function value ($f(Z)$) in order to compensate the falsification of the input data,
   - whereby the auxiliary function value ($f(Z)$) was previously determined by execution of the one or more operations (f) with the auxiliary data (Z) as input data in safe surroundings and stored on the data carrier (1) along with the auxiliary data (Z).

6. A data carrier according to claim 5, characterized in that the combination with the auxiliary function values ($f(Z)$) for compensating the falsification is performed at the latest directly before execution of an operation (g) which is non-linear with respect to the combination generating the falsification.

7. A data carrier according to either of claims 5 and 6, characterized in that the auxiliary data (Z) are varied, the corresponding auxiliary function values ($f(Z)$) being stored in the memory of the data carrier (1).

8. A data carrier according to claim 7, characterized in that new auxiliary values (Z) and new auxiliary function values ($f(Z)$) are generated by combining two or more existing auxiliary data (Z) and auxiliary function values ($f(Z)$).

9. A data carrier according to claim 8, characterized in that the existing auxiliary data (Z) and auxiliary function values ($f(Z)$) intended for the combination are each selected randomly.

10. A data carrier according to any of claims 5 to 7, characterized in that pairs of auxiliary data (Z) and auxiliary function values ($f(Z)$) are generated by a generator without the operation ($f(Z)$) being applied to the auxiliary data (Z).

11. A data carrier according to any of claims 5 to 10, characterized in that the auxiliary data (Z) are a random number.

12. A data carrier according to any of claims 5 to 11, characterized in that the combination is an EXOR operation.

13. A data carrier according to any of the above claims, characterized in that a plurality of operations can be executed with the operating program, it holding for at least a subset of said operations that the total result achieved by execution of several operations of the subset does not depend on the order of execution of the operations, and the order of execution of the stated subset of operations is varied at least when the subset contains one or more security-relevant operations.

14. A data carrier according to claim 13, characterized in that the order of execution is varied at each run through the stated subset of operations.

15. A data carrier according to claim 13 or 14, characterized in that the order of execution is varied according to a fixed principle.

16. A data carrier according to claim 13 or 14, characterized in that the order of execution is varied randomly.

17. A data carrier according to either of claims 13 and 14, characterized in that the order of execution is varied in accordance with the data processed with the operations (*f*).

18. A data carrier according to any of claims 13 to 17, characterized in that the order of execution is fixed before execution of the first operation (*f*) of the subset for all operations of the subset whose execution is intended to be directly successive.

19. A data carrier according to any of claims 13 to 18, characterized in that it is fixed before the onset of execution of an operation (*f*) of the subset which operation of the subset whose execution is intended to be successive is executed next.

20. A data carrier according to any of the above claims, characterized in that the security-relevant operations are key permutations or permutations of other secret data.

21. A data carrier according to any of the above claims, characterized in that the data carrier is a smart card.

22. A method for executing security-relevant operations in a data carrier (1) with a semiconductor chip (5) having at least one memory in which an operating program containing a plurality of commands is stored, each command causing signals detectable from outside the semiconductor chip (5), characterized in that the data carrier performs security-relevant operations (*f*) solely using operating program commands of such a kind, or using said commands in such a way, that the data processed with the corresponding commands cannot be inferred from the detected signals.

23. A method according to claim 22, characterized in that the commands used employ data present at least byte by byte.

24. A method according to either of claims 22 and 23, characterized in that the commands used are indistinguishable with respect to the signal patterns caused thereby.

25. A method according to any of claims 22 to 24, characterized in that the commands used each lead to a signal pattern which is substantially independent of the data processed with the command.

26. A method for protecting secret data serving as input data for one or more operations, characterized in that

- the input data are falsified by combination with auxiliary data (Z) before execution of the one or more operations (f),
- the output data determined by execution of the one or more operations (f) are combined with an auxiliary function value ($f(Z)$) in order to compensate the falsification of the input data,
- whereby the auxiliary function value ($f(Z)$) was previously determined by execution of the one or more operations (f) with the auxiliary data (Z) as input data in safe surroundings and stored along with the auxiliary data (Z).

27. A method according to claim 26, characterized in that the combination with the auxiliary function values ($f(Z)$) for compensating the falsification is performed at the latest directly before execution of an operation (g) which is nonlinear with respect to the compensation generating the falsification.

28. A method according to either of claims 26 and 27, characterized in that the auxiliary data (Z) are varied, the corresponding auxiliary function values ($f(Z)$) being stored in the memory of the data carrier.

29. A method according to claim 28, characterized in that new auxiliary values (Z) and new auxiliary function values ($f(Z)$) are generated by combination of two or more existing auxiliary data (Z) and auxiliary function values ($f(Z)$).

30. A method according to claim 29, characterized in that the existing auxiliary data (Z) and auxiliary function values ($f(Z)$) intended for the combination are each selected randomly.

31. A method according to any of claims 26 to 30, characterized in that pairs of auxiliary data (Z) and auxiliary function values ($f(Z)$) are generated by a generator without the operation ($f(Z)$) being applied to the auxiliary data (Z).

32. A method according to any of claims 26 to 31, characterized in that the auxiliary data (*Z*) are a random number.

33. A method according to any of claims 26 to 32, characterized in that the combination is an EXOR operation.

34. A method for executing a plurality of operations (*f*) within the operating system of a data carrier (1), it holding for at least a subset of said operations that the total result achieved by execution of several operations of the subset does not depend on the order of execution of the operations, and the order of execution of the stated subset of operations is varied at least when the subset contains one or more security-relevant operations.

35. A method according to claim 34, characterized in that the order of execution is varied at each run through the stated subset of operations.

36. A method according to claim 34 or 35, characterized in that the order of execution is varied according to a fixed principle.

37. A method according to claim 34 or 35, characterized in that the order of execution is varied randomly.

38. A method according to either of claims 34 and 35, characterized in that the order of execution is varied in accordance with the data processed with the operations (*f*).

39. A method according to any of claims 34 to 38, characterized in that the order of execution is fixed before execution of the first operation of the subset for all operations of the subset.

40. A method according to any of claims 35 to 39, characterized in that it is fixed before the onset of execution of an operation (*f*) of the subset which operation of the subset whose execution is intended to be successive is executed next.

41. A method according to any of claims 22 to 40, characterized in that the security-relevant operations are key permutations or permutations of other secret data.

Abstract

The invention relates to a data carrier (1) having a semiconductor chip (5). In order to prevent an attacker from determining secret data of the chip (5) from intercepted signal patterns of the chip (5), security-relevant operations are performed only with commands or command strings of the operating program whose use does not permit the processed data to be inferred from the signal patterns.

FIG.1

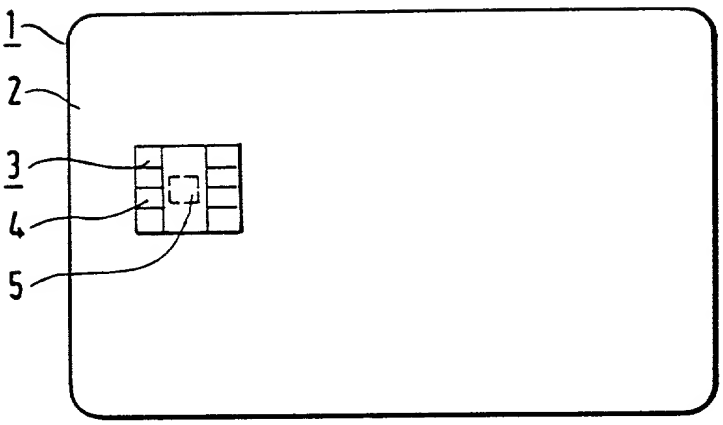


FIG.2

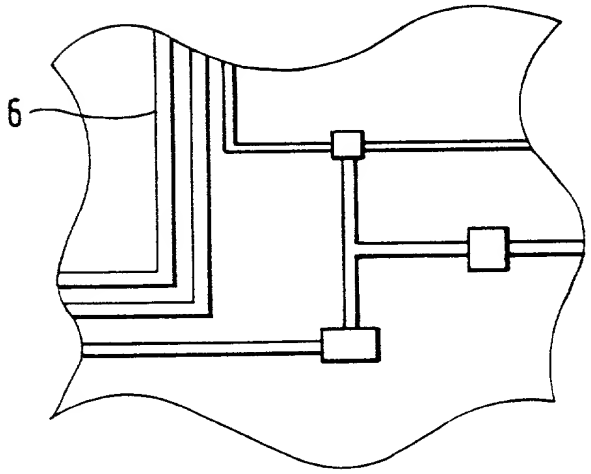


FIG.3

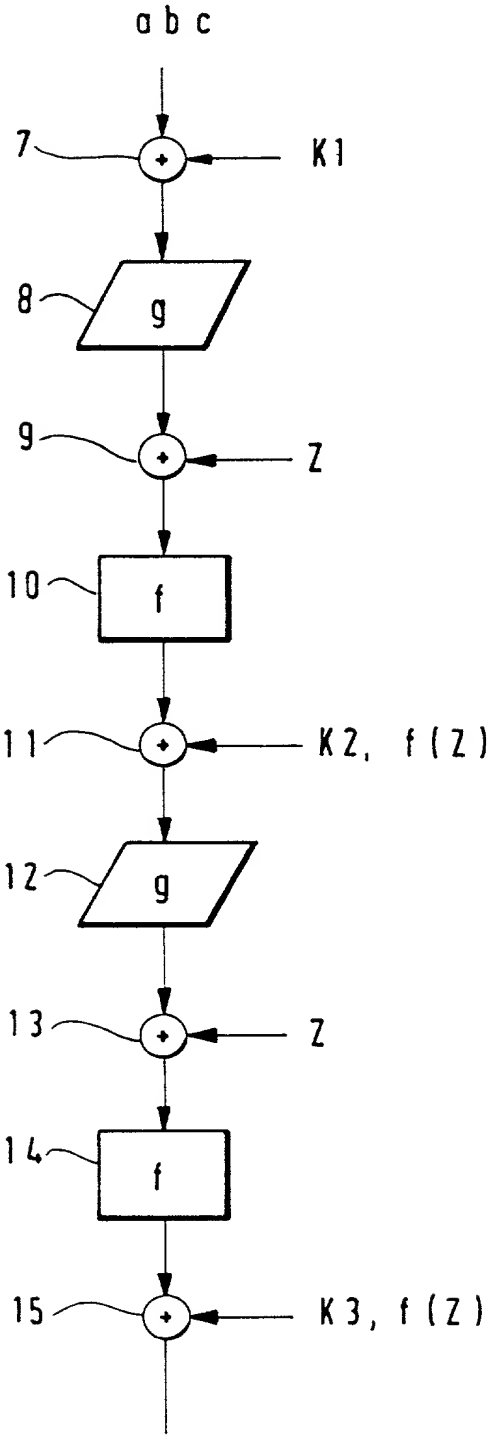


FIG. 4

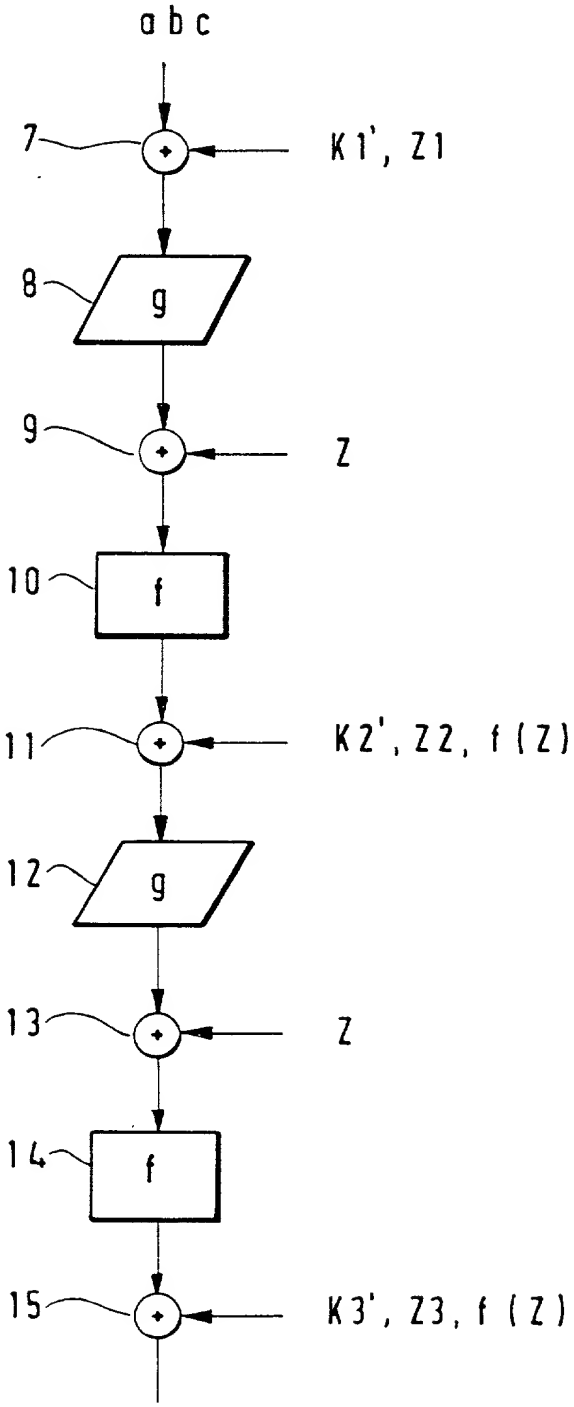
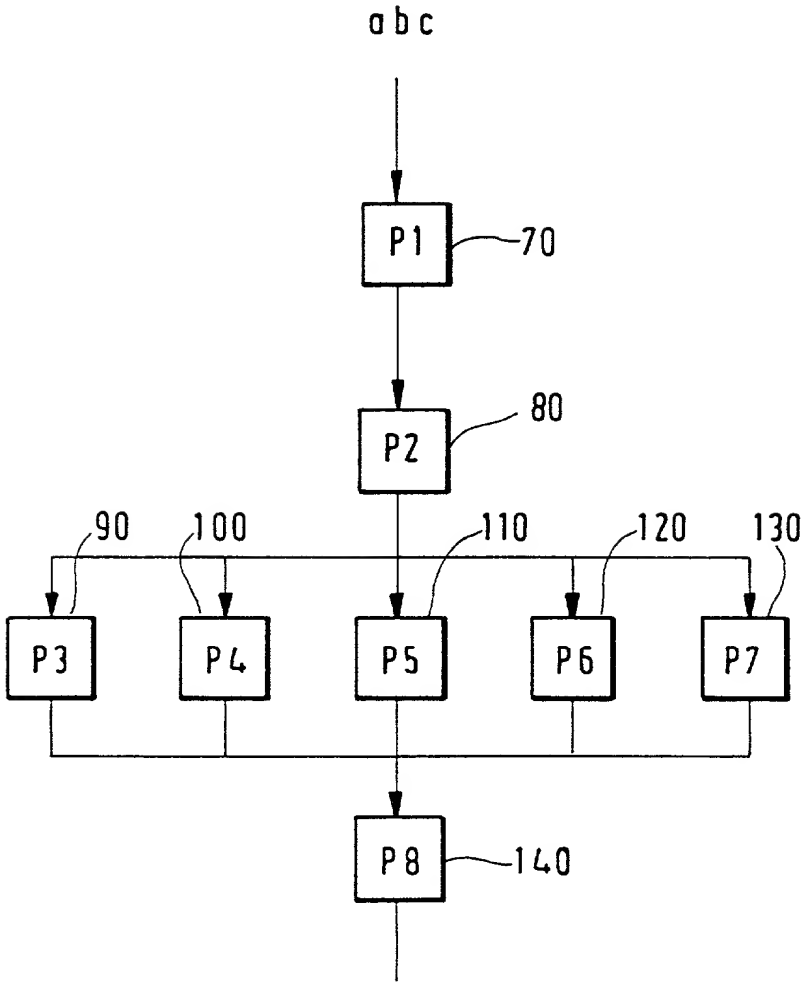


FIG.5



ATTORNEY/DOCKET NO **JEK/Vater**

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

ACCESS-CONTROLLED DATA STORAGE MEDIUM

the specification of which (check one):

☐ is attached hereto, or ☒ was filed on: **17 November 2000** as U S Application Number or PCT International Application Number: **(PCT/EP99/03385) 09/700,656**

and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56*. I hereby claim foreign priority benefits under *Title 35, United States Code §119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	**Country**	**Day/Month/Year Filed**	**Yes**	**No**
198 22 217.3	Germany	18 May 1998	X	
198 22 220.3	Germany	18 May 1998	X	
198 22 218.1	Germany	18 May 1998	X	

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE §119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.

Application Number	Day/Month/Year Filed

☐ Additional Provisional Application(s) Listed on Following Page(s)

I hereby claim the benefit under *Title 35, United States Code, §120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code, §112*, I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

☐ Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

POWER OF ATTORNEY I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith J Ernest Kenney, Reg No. 19,179 Eugene Mar, Reg. No. 25,893, Richard E Fichter, Reg No. 26,382, Thomas J Moore, Reg No. 28,974, Joseph DeBenedictis, Reg No. 28,502, Benjamin E. Urcia, Reg No. 33,805; and

I(we) authorize my(our) attorneys to accept and follow instructions from **Klunker Schmitt-Nilson Hirsch** regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I(we) or my(our) assigns withdraw this authorization in writing.

Send correspondence to: **BACON & THOMAS, PLLC**
625 Slaters Lane - 4th Floor
Alexandria, VA 22314-1176

Telephone Calls to: **J. Ernest Kenney (703) 683-0500**

FULL NAME OF FIRST OR SOLE INVENTOR	CITIZENSHIP
Harald VATER	**Germany**
RESIDENCE ADDRESS An den Schulgarten 23, D-35398 Giessen, Germany	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW
DATE Jan. 22, 2001	SIGNATURE Harald Vater

☒ *See following page(s) for additional joint inventors.*

CONTINUATION OF DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

PRIOR FOREIGN APPLICATION(S) (35 USC §119)			PRIORITY CLAIMED	
Number	**Country**	**Day/Month/Year Filed**	**Yes**	**No**

PRIOR PROVISIONAL APPLICATIONS 35 U.S. CODE §119(E)	
Application Number	**Day/Month/Year Filed**

PRIOR U.S. OR PCT INTERNATIONAL APPLICATIONS (35 U.S. CODE §120)		
Application Number	**Filing Date**	**Status - Patented, Pending or Abandoned**

FULL NAME OF JOINT INVENTOR	CITIZENSHIP
200 **Hermann DREXLER**	**Germany**
RESIDENCE ADDRESS Oberlanderstrasse 5a, D-81371 Munchen, Germany DEX	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW
DATE Jan. 22, 2001	SIGNATURE

FULL NAME OF JOINT INVENTOR	CITIZENSHIP
300 **Eric JOHNSON**	**Great Britain**
RESIDENCE ADDRESS Gaissacher Strasse 7, D-81371 Munchen, Germany DEX	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW Eric Johnson
DATE 26 Jan 2001	SIGNATURE

FULL NAME OF JOINT INVENTOR	CITIZENSHIP
RESIDENCE ADDRESS	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW
DATE	SIGNATURE

FULL NAME OF JOINT INVENTOR	CITIZENSHIP
RESIDENCE ADDRESS	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW
DATE	SIGNATURE

☐ *See following pages for additional joint inventors/priority applications.*